Overview of SINAP Timing System

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Outline

• System design
• Hardware modules
• Performance
• Application
• Future plan
10-year history

- **Sep. 2007**: Development began.
- **Aug. 2010**: 1st test on site succeeded @ PLS-II
- **Dec. 2014**: Standalone modules for Brazil Sirius delivered.
- **Mar. 2015**: Development of femtosecond timing system began.
- **Jun. 2016**: Implemented at damping ring of SuperKEKB.
SINAP v1 timing system structure

**VME 6U module; A16D32 addressing**
- **Input:** 1ch RF clock (0 – 10 dBm)
- 1ch AC line (0Vp-p typical)
- **Output:** 1ch multi-mode fiber
  - 1ch Sequence RAM trigger (TTL)

**VME 6U module**
- **Input:** 1ch multimode fiber
- **Output:** 12ch multimode fiber
SINAP v2 timing system structure
Hardware structure of v2 system

- “Jitter cleaning” is not adopted;
- No local oscillator or DDS.

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**Hardware Components**

- **EVO configured as EVG**
  - Uplink: SFP → GTX
  - Recovery clock: GTX → event FIFO
  - Data FIFO: event FIFO → data Switching
  - AC line: data Switching → RF clock
  - Downlink: data Switching → SFP0, SFP1, ..., SFP7, GTX0, GTX1, ..., GTX7

- **EVO configured as EVR**
  - Uplink: SFP → GTX
  - Recovery clock: GTX → EVR logic
  - Data logic: EVR logic → data Switching
  - Downlink: data Switching → STD-OE, STD-OE, ..., STD-OE, GTX0, GTX1, ..., GTX7

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Hardware modules

• Product list

<table>
<thead>
<tr>
<th>No.</th>
<th>Module</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VME-EVO</td>
<td>Configured as EVG or EVR or FOUT, 1ch SFP in, 8ch SFP out</td>
</tr>
<tr>
<td>2</td>
<td>VME-EVE</td>
<td>Configured as EVR, 1ch SFP in, 8ch TTL out</td>
</tr>
<tr>
<td>3</td>
<td>VME-FOUT</td>
<td>1ch SFP in, 12ch SFP out</td>
</tr>
<tr>
<td>4</td>
<td>VME-MOE</td>
<td>4ch SFP in, 4 TTL(5V) out</td>
</tr>
<tr>
<td>5</td>
<td>PLC-EVR</td>
<td>1ch SFP in, 4 TTL out</td>
</tr>
<tr>
<td>6</td>
<td>STD-EVO</td>
<td>Configured as EVG or EVR or FOUT, 1ch SFP in, 8ch SFP out @ front panel, XportPro for embedded IOC, 12ch 1528 out or 16ch TTL out @ rear panel</td>
</tr>
<tr>
<td>7</td>
<td>STD-EVE</td>
<td>Configured as EVR, 1ch SFP in, 8ch TTL out @ front panel, XportPro for embedded IOC, 12ch 1528 out or 16ch TTL out @ rear panel</td>
</tr>
<tr>
<td>8</td>
<td>STD-MOE</td>
<td>1ch SFP in, 12ch SFP out</td>
</tr>
<tr>
<td>9</td>
<td>STD-SOE</td>
<td>2ch 2528 in, 2ch TTL(5V) out, 8 interlock in</td>
</tr>
<tr>
<td>10</td>
<td>SOE</td>
<td>1ch 2528 in, 1ch TTL(5V) out, 1 interlock in</td>
</tr>
</tbody>
</table>
Hardware modules

Configured to EVG, EVR or FANOUT by software
VME 6U module, A16D32 addressing
Input: 1 RF clock (0 – 10dBm)
1 interlock / AC-line (TTL)
1 fiber (SFP module)
Output: 8 fiber (SFP module)

Yokogawa FAM3 series, 1-slot module
Input / Output register mode
External 5V/3A DC power supply is required
Input: 1 fiber (SFP module)
Output: 4 outputs (TTL)

Configured to EVR
VME 6U module, A16D32 addressing
Input: 1 interlock (TTL)
1 fiber (SFP module)
Output: 8 outputs (TTL)
1 RF recovery clock

19 inches 1U standard chassis
110/220V 50-60Hz AC power supply
Input: 4 fiber (SFP module)
Output: 4 outputs (TTL)

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Hardware modules

• Standalone version of EVO and EVE
  – EVO can be configured as EVG, EVR or Fanout, 1ch SFP in, 8ch SFP out, 12ch 1528 out or 16ch TTL out;
  – EVE can be configured as, 1ch SFP in, 8ch TTL out, 12ch 1528 out or 16ch TTL out;
  – Xport PRO mounted to serve as an embedded IOC.
Software

• VME modules
  – Support vxWorks 5.5 & vsWorks 6.x
  – EPICS 3.14.x

• Standalone modules
  – Embedded IOC
  – μcLinux 2.6.30.4
Performance

- Stability

coding-decoding error

![Diagram showing VME chassis, EVG output, EVR output, counter, fiber, RF clock, AC line, and EVG.]

![Image of Count Panel showing Count A: 728942, Count B: 728942, and Runtime: 101.34 hours.]

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SINAP
Shanghai Institute of Applied Physics, Chinese Academy of Sciences
Performance

- Jitter-v1
  \(~ 10\text{ps}\)

- Jitter-v2
  \(~ 6\text{ps}\)
Performance

• Phase Shift

Phase shift with temperature changing (35ps/°C)
Application

• Timing system for large accelerator facilities.

PLS-II@Korea

SSRF@China

SuperKEKB@Japan

CSNS@China

ADS@China

Sirius@Brazil
Application

• PLS-II @ Korea
Application

- SuperKEKB @ Japan
  - The LINAC chose $2856 \div 25=114.24\text{MHz}$ as RF clock, while main ring and damping ring chose 508.9MHz as RF frequency.
  - Timing system of LINAC and timing system of main ring should be locked.

Bucket Selection at SuperKEKB

We choose harmonic number of 230 so that 23 kinds of combination between DR and MR are made.

The delay time of 0 – 11.34\text{ms} (=493\text{ms} \times 23) is needed when we control both DR-bucket and MR-bucket with the same method.
Application

- SuperKEKB @ Japan
  - EVG cascading function is utilized in EVO module for main ring timing system.
  - Logic in FPGA of EVO locks the two frequency, so timing of LINAC and timing of main ring are also locked.
Application

• SuperKEKB @ Japan

Hiroshi Kaji, Kazuro Furukawa, Masako Iwasaki et al.
Application

• Sirius @ Brazil
Application

- Shanghai Proton Therapy Facility
  - Timing system
  - Irradiation control system
Application

- Shanghai Proton Therapy Facility
  - timing system
Application

• Shanghai Proton Therapy Facility
  – Irradiation control system
    • 2 EVO configured as irradiation controller and irradiation monitor, respectively;
    • Send events to upstream EVG to execute spot-scanning irradiation;
    • Receive dose and position data of beam from ionization chambers in nozzle;
    • Receive scanning magnet field data, control scanning magnets in nozzle;
    • Control snout movement;
    • Interact with interlock system.
Future plan

- Development of femtosecond timing system
  - The short-term jitter of the transmitted RF signal: 10fs;
  - The long-term drift: 40fs.
Future plan

- Integrate event timing system to the femtosecond timing system.
  - The generator transmits modulated RF reference and event stream through one fiber;
  - The fanout distributes RF reference and event stream, and compensates phase drift of uplink;
  - The receiver compensates phase drift of uplink, and recovers electric RF reference and optical event stream;
  - EVR modules in μTCA chassis output stabilized clocks and triggers.
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THANKS.

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